REMARKS

Reconsideration of the objections and rejections of the claims is respectfully requested on the basis of the following particulars.

1. Claim Objection

This rejection has been addressed in the amendment to claim 2 by further defining the "front side" as being disposed in a thickness direction of the substrate, and replacing the term "backside" with "rear side" and further defining the rear side as being opposite to the front side. Removal of this rejection is thus requested.

2. Rejection of claims 1-8 under 35 U.S.C. 112, first paragraph

This rejection has been addressed by removing the term "simultaneously" from claim 1 and replacing this term with the expression "while." Applicant submits that by using the term "while," the subject matter of claim 1 is readily ascertainable in view of the specification in the present application. In view of this amendment, withdrawal of this rejection is respectfully requested.

3. Rejection of claims 1-4 and 8 under 35 U.S.C. 102(b) as being anticipated by Finnila (U.S. Patent 5,426,072)

Claims 1-4 and 8 stand rejected as being anticipated by the teachings of Finnila. In view of the amendment to the claims and the foregoing remarks, Applicant respectfully traverses this rejection on the basis that Finnila fails to disclose or suggest a method for producing a vertically integratable circuit having electrically conductive contacts for vertical integration while producing the electrically conductive contacts for vertical integration and the integrated circuit itself. Claims 1 and 2 are therefore patentable. Claims 3-4 and 8, which depend directly or directly from claim 1, are also patentable based on their dependency from claims 1 and 2 and their individually recited method steps.

a. Invention Summarized

In the present invention, as recited in claim 1, a method for producing vertically integratable circuits is provided that includes producing electrically conductive contacts for vertical integration while producing the integratable circuits themselves, electrically conductive contacts for vertical integration and electrically conductive contacts of the integrated circuit in a continuous process.

The method recited in claim 2 comprises the following steps:

a) producing an insulation at the places of the contacts for vertical integration on a front side in a thickness direction of a substrate bearing the vertically integratable circuits,

b) producing a gap within the insulations from the front side,

c) filling the gaps with an electroconductive material from the front side to form at least some of the contacts,

d) exposing the electroconductive material from a rear side opposite the front side of the substrate bearing the vertically integratable circuits at the places of the contacts for vertical integration, and

e) applying an electroconductive material from the rear side to the previously exposed electric material at the places of the contacts for vertical integration to form at least some of the contacts.

b. Reference Distinguished

While Finnila teaches a process for manufacturing an integratable circuit, this reference teaches a process different than the process recited in claims 1 and 2 of the present invention on the basis of the following particulars.

Firstly, in observing FIGS. 2-5, Finnila describes that an insulating layer 13 to the silicone film 12 is applied before the circuitry 17, 18 of the integrated circuit is provided onto the silicone film 12 (col. 3, lines 45-49, 56 through col. 4, line 4). On the other hand, it will be pointed out that in step (a) of the method of claim 2 of the present invention, an insulating layer is applied to the front side of a substrate already bearing a vertically integratable circuit. Since the insulating layer is applied before the circuitry in Finnila, the feedthroughs 16 are also formed before the circuitry is provided. Once again, in the present invention, such feedthroughs or gaps are formed after the circuitry is provided onto the substrate, as recited in step (b) of claim 2.

Next, Finnila describes a different method for forming the electrically conductive contacts than in the present invention, as recited in claims 1 and 2. As shown in FIG. 4, the method of Finnila first includes depositing electrically conductive member 16a within the feedthroughs. Unlike in the present invention wherein the electroconductive material deposited in the gaps formed in the insulating layer comprises the electrically conductive contacts for vertical integration, the electrically conductive member 16a according to Finnila does not form the contacts for vertical integration. Instead, as shown in FIG. 5, Finnila further includes the step of depositing another silicone layer 20 over the circuitry 18 and then forming yet another series of openings with metalization 21 deposited therein so as to contact the conductive feedthroughs (col. 4, lines 36-38). After the metalization 21 is formed, an overglass layer is then deposited over the silicone layer 20 and openings are formed in which indium bumps 23 are provided to contact the metalization 21 (col. 4, lines 46-49).

It appears, therefore, that the electrically conductive contacts for vertical integration and of the integrated circuit are not produced in a continuous process, as recited in claim 1 of the present invention. This is due to the fact that the indium bumps and the metalization are formed in a post-production process after the

electrically conductive member 16a and the integrated circuit are formed. Accordingly, Finnila describes a method in which the integrated circuit is adapted to be vertically integratable only after it is already formed and is not rendered vertically integratable while it is being formed in a continuous process as recited in claim 1.

As shown in FIG. 7 of Finnila, it appears necessary that the indium bumps 23 be provided on the vertically integratable circuit of Finnila (col. 6, lines 31-36). As indicated in col. 6, lines 34-36, Finnila states that the structure 1 can be any suitable silicone or SOI wafer having circuitry and interconnecting bumps on the top surface. Accordingly, the indium or interconnecting bumps in Finnila are essential to the vertically integratable circuit itself. On the other hand, the method for forming the vertically integratable circuit of the present invention recited in claims 1 and 2 do not include indium bumps and instead the electrically conductive contacts are formed by only having electroconductive material filled in the gaps formed on the substrate.

In view of these observations, Applicant submits that Finnila fails to disclose or suggest the method of the present invention as recited in claims 1 and 2. Accordingly, withdrawal of the rejection of claims 1-4 and 8 is respectfully requested.

4. Rejection of claims 5, 9 and 10 under 35 U.S.C. 103(a) as being unpatentable over Finnila (U.S. Patent 5,426,072)

Claims 5, 9 and 10 stand rejected as being unpatentable over Finnila. Applicants traverse this rejection with regards to claim 5 in view of the aforesaid comments regarding claims 1 and 2.

In view of claims 9 and 10, Applicant has amended claim 9 by reciting that the electrically conductive contacts have exposed end portions that are disposed along front and rear sides in a thickness direction of the vertically integratable circuit. In view of this amendment, Applicant respectfully traverses the rejection of these claims in view of Finnila. Particularly, as indicated above in reference to claims 1 and 2, the vertically integratable circuit of Finnila includes a plurality of indium bumps

along the front and rear surfaces thereof. These indium bumps are not the electrically conductive contacts that form part of the vertically integrated circuit of Finnila, but instead, as shown in FIG. 5, connect to the metalization 21 and the electrically conductive member 16a within the feedthroughs 16. Accordingly, even if the metalization or the electrically conductive members are construed as the electrically conductive contacts, as is done in the Office Action, the metalization and electrically conductive members are not exposed and instead, are covered by the layer 20 and the indium bumps 23.

Accordingly, in view of these observations on Finnila, Applicant submits that Finnila fails to disclose, teach or suggest the vertically integratable circuit recited in claims 9 and 10 of the present invention. Withdrawal of this rejection is therefore requested.

5. Rejection of claim 6 under 35 U.S.C. 103(a) as being unpatentable over Finnila (U.S. Patent 5,426,072) in view of Silicon Processing for the VLSI Era (Wolf et al.)

Claim 6 stands rejected in view of the teachings of Finnila and Wolf et al. Claim 6 directly depends from claim 2. Applicants respectfully traverse this rejection on the basis that the teachings of Wolf et al. fail to make up for the basic shortcomings discussed above in reference to the rejection of claims 1 and 2 in view of the teachings of Finnila. Specifically, the teachings of Wolf et al. fail to disclose or suggest the step of applying insulation and forming electrically conductive contacts to a substrate bearing the vertically integratable circuit. In view of this observation, Applicant submits that the teachings of Finnila and Wolf et al., whether considered collectively or individually, fail to disclose or suggest the basic method of claims 1 and 2. Accordingly, claim 6 is at least patentable based on its dependency from claim 2. Withdrawal of the rejection is therefore requested.

6. Rejection of claim 7 under 35 U.S.C. 103(a) as being unpatentable over Finnila (U.S. Patent 5,426,072) in view of Semiconductor Manufacturing Technology (Quirk et al.)

Claim 7 stands rejected in view of the teachings of Finnila and Quirk et al. Claim 7 directly depends from claim 2. Applicants respectfully traverse this rejection on the basis that the teachings of Quirk et al. fail to make up for the basic shortcomings discussed above in reference to the rejection of claims 1 and 2 in view of the teachings of Finnila. Specifically, the teachings of Quirk et al. fail to disclose or suggest the step of applying insulation and forming electrically conductive contacts to a substrate bearing the vertically integratable circuit. In view of this observation, Applicant submits that the teachings of Finnila and Quirk et al., whether considered collectively or individually, fail to disclose or suggest the basic method of claims 1 and 2. Accordingly, claim 7 is at least patentable based on its dependency from claim 2. Withdrawal of the rejection is therefore requested.

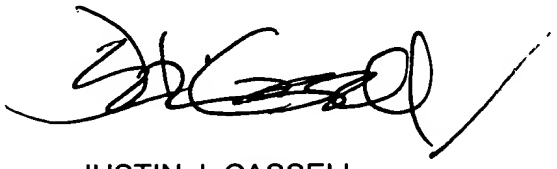
7. Conclusion

In view of the amendment to the claims, and further in view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is respectfully requested that claims 1-10 be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the Applicant's' Attorney, the Examiner is invited to contact the undersigned at the numbers shown below.

BACON & THOMAS, PLLC
625 Slaters Lane, Fourth Floor
Alexandria, Virginia 22314-1176
Phone: (703) 683-0500

Respectfully submitted,



Date: July 31, 2003

JUSTIN J. CASSELL
Attorney for Applicant
Registration No. 46,205

S:\Producer\jek\GRASSL - 926377\amendment.wpd